IN THE CLAIMS:

1-25. (canceled)

26. (new) A buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising:

an inverter stage input;

an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output;

a buffered field effect transistor logic (BFL) stage coupled to the inverted output and comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel, and a voltage drop circuit electrically connected in series between said first channel and said second channel;

a first output at an electrical node between said voltage drop circuit and said first channel, wherein said circuit is fabricated on a silicon carbide substrate; and

a second output at an electrical node between said voltage drop circuit and said second channel.

27. (new) A circuit in accordance with Claim 26, wherein said first output is configured couple to a chopping circuit configured to chop a signal based on a signal received at said first output.

28. (new) A buffered field effect transistor logic (BFL) level-shifting/inverter circuit comprising:

an inverter stage input;

an NMOS depletion mode inverter responsive to said inverter stage input to produce an inverted output;

a buffered field effect transistor logic (BFL) stage responsive to said inverted output, said BFL stage comprising a first NMOS depletion mode field effect transistor (FET) having a first gate and an associated first channel, a second NMOS depletion mode FET having a second gate and an associated second channel; and a resistor electrically connected in series between said first channel and said second channel;

a first output at an electrical node between said resistor and said first channel; and

a second output at an electrical node between said resistor and said second channel, wherein said circuit is fabricated on a silicon carbide substrate.

29. (new) A circuit in accordance with Claim 28 configured to operate with a negative direct current (DC) bias on each said gate with respect to each said associated channel.